What is claimed is:

1. A semiconductor memory device comprising:

a substrate;

a MOS (metal oxide semiconductor) transistor formed in a surface portion of said substrate, wherein said MOS transistor includes a source, a gate, and a drain;

a first inter-level dielectric covering said MOS transistor;

a capacitor element including:

a bottom electrode,

a dielectric layer formed on said bottom electrode, and

an upper electrode formed on said dielectric layer;

a first contact formed through said first inter-level dielectric to electrically connect said bottom electrode to said source, wherein said first contact includes a first metal portion formed of metal.

2. The semiconductor memory device according to claim 1, wherein said metal is refractory metal, and said first contact further includes a barrier layer formed between said source and said first metal portion.

3. The semiconductor memory device according to claim 2, wherein said refractory metal is tungsten, and said contact barrier layer is formed of titanium nitride.

4. The semiconductor memory device according to claim 3, wherein said bottom electrode includes:

a polysilicon layer connected to said dielectric layer, and

an electrode barrier layer formed between said first metal portion and said polysilicon layer.

5. The semiconductor memory device according to claim 4, wherein said electrode barrier layer is formed of titanium nitride.

6. The semiconductor memory device according to claim 1, further comprising:

a second contact formed through said first inter-level dielectric to be connected to said drain, wherein said second contact includes a second metal portion formed of said metal.

7. The semiconductor memory device according to claim 6, wherein said metal is tungsten, and

said second contact further includes a second barrier layer formed of titanium nitride between said drain and said second metal portion.

8. The semiconductor memory device according to claim 6, further comprising:

a second inter-level dielectric covering said capacitor element and said first inter-level dielectric;

a third contact formed through said second inter-level dielectric; and

a bit line formed on said second inter-level dielectric, wherein said second and third contact electrically connect said drain to said bit line.

9. The semiconductor memory device according to claim 8, further comprising:

another MOS transistor provided in a surface portion of said substrate for a peripheral circuit;

a fourth contact formed through said first inter-level dielectric to be connected to said another MOS transistor on a source/drain thereof;

a fifth contact formed through said second inter-level dielectric to be connected to said fourth contact, wherein said fourth contact

includes a third metal portion formed of said metal.

10. The semiconductor memory device according to claim 1, wherein said bottom electrode comprises:

a polysilicon layer connected to said dielectric layer, and

an electrode barrier layer formed between said first metal portion and said polysilicon layer.

11. The semiconductor memory device according to claim 10, wherein said electrode barrier layer is formed of titanium nitride.

12. The semiconductor memory device according to claim 10, further comprising a second inter-level dielectric covering said first inter-level dielectric, wherein a hole is formed through said second inter-level dielectric, and

wherein said electrode barrier layer includes:

a bottom barrier portion formed on said metal portion of said first contact, and

a side barrier portion connected to said bottom barrier portion, said side barrier portion

being formed on a side surface of said hole to extend towards an upper surface of said second inter-level dielectric, and wherein

said polysilicon layer includes:

a bottom electrode portion formed on said bottom barrier portion, and

a side electrode portion connected to said bottom electrode portion, said side electrode portion being formed on said side barrier portion, and

wherein an end of said side electrode portion is substantially in alignment with said upper surface of said second inter-level dielectric, while an end of said side barrier portion is out of alignment with said upper surface of said second inter-level dielectric, said side barrier portion not reaching said upper surface of said second inter-level dielectric.

13. A method of fabricating a semiconductor memory device comprising:

providing a substrate;

forming a MOS transistor in a surface portion of said substrate, wherein said MOS transistor includes a gate, a source, and a drain;

forming a first inter-level dielectric to

cover said MOS transistor;

forming a first contact through said first inter-level dielectric such that said first contact is connected to said source of said MOS transistor, wherein said first contact includes a first metal portion formed of metal;

forming a bottom electrode connected to said first contact;

forming a dielectric layer formed on said bottom electrode;

forming an upper electrode formed on said dielectric layer.

14. The method according to claim 13, wherein said metal of said first metal portion is refractory metal, and said first contact further includes a first contact barrier layer formed between said source and said first metal portion.

15. The method according to claim 14, wherein said refractory metal is tungsten, and said contact barrier layer is formed of titanium nitride.

16. The method according to claim 13, wherein said bottom electrode includes:

a polysilicon layer connected to said

dielectric layer, and

an electrode barrier layer formed between said first metal portion and said polysilicon layer.

17. The method according to claim 16, wherein said metal is tungsten and said electrode barrier layer is formed of titanium nitride.

18. The method according to claim 13, further comprising:

forming a second inter-level dielectric to cover said first inter-level dielectric and said first contact;

forming a hole through said second inter-level dielectric to expose said first contact,

wherein said forming said bottom electrode includes:

depositing a conductive barrier material film on a side surface and bottom surface of said hole,

depositing a polysilicon film on said conductive barrier material film,

concurrently removing outside portions of said conductive barrier material film and said polysilicon film outside said hole to form said electrode barrier layer and said polysilicon

layer, and

selectively etching an end portion of said electrode barrier layer in the vicinity of an upper surface of said second inter-level dielectric such that an end of said conductive barrier material film does not reach said upper surface of said second inter-level dielectric, while said polysilicon layer is not etched.

19. The method according to claim 18, further comprising:

forming a resist layer on said polysilicon film to plug said hole after said depositing said polysilicon film, wherein said layer is used as a mask for said concurrently etching; and

removing said resist layer by a plasma process in an atmosphere including fluorocarbon, wherein said selectively etching is concurrently achieved during said removing said resist layer.

20. The method according to claim 13, further comprising:

forming an etching stopper layer to cover said first contact and said first inter-level dielectric;

forming a second inter-level dielectric on said etching stopper layer;

etching said second inter-level dielectric to expose a portion of said etching stopper layer, wherein said etching said second inter-level dielectric is stopped by said etching stopper layer;

etching said etching stopper layer to said first contact to form a hole penetrating said second inter-level dielectric and said etching stopper layer, wherein said bottom electrode, said dielectric layer, and said upper electrode are disposed inside said hole.

21. The method according to claim 13, further comprising:

forming a second contact formed through said first inter-level dielectric to be connected to said drain, said second contact including a second metal portion formed of said metal, wherein said first and second contacts are concurrently formed; and

forming a bit line, wherein said bit line is electrically connected to said drain through said second contact.

22. The method according to claim 21, further comprising:

forming another MOS transistor in a surface

portion of said substrate for a peripheral circuit;

forming a third contact formed through said first inter-level dielectric to be connected to a source/drain region of said another MOS transistor, said third contact including a third metal portion formed of said metal, wherein said first, second and third contacts are concurrently formed; and

forming an interconnection, wherein said interconnection is electrically connected to said source/drain region through said third contact.